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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,868	12/29/2003	Jong-Soo Choi	9898-319	3708

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EXAMINER	
BEVERIDGE, RACHEL E	
ART UNIT	PAPER NUMBER
1725	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,868	CHOI ET AL.	
	Examiner	Art Unit	
	Rachel E. Beveridge	1725	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) *10 and 11* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-11* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election without traverse of claims 1-9 in the reply filed on January 12, 2006 is acknowledged.

Applicant's arguments filed January 12, 2006 have been fully considered but they are not persuasive. Applicant believed that the restriction between claims 1-9 and newly amended claim 11 is not necessary. The examiner disagrees. Claim 11, drawn to "a printed circuit board made by using the method of claim 1," is still claiming the originally restricted product with the addition of the intended use limitation regarding the method of claim 1. Furthermore, the applicant's election without traverse does not include traversal of non-elected claims.

Drawings

The informal drawings are not of sufficient quality to permit examination. Accordingly, replacement drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to this Office action. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action.

Applicant is given a TWO MONTH time period to submit new drawings in compliance with 37 CFR 1.81. Extensions of time may be obtained under the provisions

of 37 CFR 1.136(a). Failure to timely submit replacement drawing sheets will result in ABANDONMENT of the application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 and 4-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson et al. (US 5,394,609) in view of Chiang (US 5,676,561).

With respect to claims 1 and 4-9, Ferguson discloses a method of populating printed circuit boards with surface mount technology devices (Ferguson, abstract, lines 1-2). Ferguson shows a printed circuit board (11) with an interface for connection (21) in figure 1. Ferguson teaches selectively applying solder onto contact pads on the surfaces of each of the printed circuit boards (Ferguson, col. 6, lines 17-18) which include an interconnect (21) (Ferguson, col. 6, line 2). Ferguson also discloses the solder application is done through a screen (Ferguson, col. 6, lines 22-23) in one or more solder reflow cycles (Ferguson, col. 6, lines 8-11). Figure 5, step 2 refers to screen soldering the first side of the interconnect (21), whereas figure 5, step 9 refers to screen soldering the second side of the interconnect (21) on the printed circuit board (11). Figure 5, step 4 refers to reflowing the solder on the first side of the interconnect (21); whereas, figure 5, step 11 refers to reflowing the solder on the second side of the

interconnect (21) on the printed circuit board (11), and Ferguson discloses following the reflow step with a cooling step to solidify the solder and connection (Ferguson, col. 6, line 66). Furthermore, Ferguson discloses placing integrated circuit chips (25) onto the solder bearing surface of the printed circuit boards with the contact leads of the integrated circuit chips bearing on the deposited solder (Ferguson, col. 6, lines 34-37). Figure 5, steps 2-4 shows the screen soldering process followed by application of the technology devices and further reflowing the connection on the first side of the printed circuit board. Figure 5, steps 9-11 shows the screen soldering process followed by application of the technology devices and further reflowing the connection on the second side of the printed circuit board. However, Ferguson does not disclose specifically mounting pin connectors. Chiang displays a pin connector in figure 3 and teaches the connector to have a slot with a longitudinal axis for receiving an integrated circuit card in an electrically operative relationship (Chiang, col. 2, lines 4-8). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the method of Ferguson to include the connection to the pin connector of Chiang in order to provide a terminal that provides good electrical connection between the primary printed circuit board and an integrated circuit card (Chiang, col. 1, lines 61-64).

Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson et al. (US 5,394,609) and Chiang (US 5,676,561) as applied to claim 1 above, and further in view of Ishikawa (JP 62203669 A).

With respect to claim 2, Ferguson discloses placing integrated circuit chips (25) onto the solder bearing surface of the printed circuit boards with the contact leads of the

integrated circuit chips bearing on the deposited solder (Ferguson, col. 6, lines 34-37). Chiang displays a pin connector in figure 3 and teaches the connector to have a slot with a longitudinal axis for receiving an integrated circuit card in an electrically operative relationship (Chiang, col. 2, lines 4-8). However, Ferguson and Chiang lack disclosure of flux covering the solder before reflow. Ishikawa discloses coating a flux after soldering the solder of both faces of the printed circuit board (Ishikawa, abstract, purpose). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined invention of Ferguson and Chiang to include the flux of Ishikawa in order to facilitate soldering at later stages by preventing the oxidation of the printed circuit board (Ishikawa, abstract, purpose).

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ferguson et al. (US 5,394,609) and Chiang (US 5,676,561) as applied to claim 1 above, and further in view of Pasch (US 5,489.804).

With respect to claim 3, Ferguson and Chiang do not discloses covering the junction area of a pin connector with flux prior to soldering the connector to the compliment junction on a printed circuit board. Pasch discloses that it is common practice in the art to apply flux "to the face of the chip and/or substrate" and that both are held at elevated temperatures to effect soldering of the two (Pasch, col. 1, lines 35-38). Pasch discloses applying flux on the surface of both the chip and the substrate at the intended points of contact (Pasch, col. 1, lines 32-35). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combined

invention of Ferguson and Chiang to include the substrate surface coated with flux of Pasch in order to effectively solder the components (Pasch, col. 1, lines 30-40).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Rachel E. Beveridge whose telephone number is 571-272-5169. The examiner can normally be reached on Monday through Friday, 9 am to 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Patrick Ryan can be reached on 571-272-1292. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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JONATHAN JOHNSON
PRIMARY EXAMINER